REMARKS

By this Amendment, Applicants add new claim 21.

Accordingly, claims 1-21 remain pending in the application.

Once again, the Examiner is respectfully requested to state whether the drawings are acceptable.

Reexamination and reconsideration are respectfully requested.

35 U.S.C. § 102

The Office Action rejects claims 1-3 and 16-20 under 35 U.S.C. § 102 over Williams et al. U.S. Patent 5,485,027 ("Williams"). Applicants respectfully traverse those rejections for at least the following reasons.

Claim 1

Among other things, the array of claim 1 includes N DMOS transistors laterally arranged in a epitaxial layer, wherein the N DMOS transistors share in common either a source or a drain.

Applicants respectfully submit that Williams does not disclose N DMOS transistors laterally arranged in an epitaxial layer, sharing either a source or a drain.

The Office Action cites FIG. 9B as showing an arrangement where a common source is employed in an N channel pull-up device.

Applicants respectfully submit that the Examiner has apparently misunderstood claim 1 and the Williams reference.

Claim 1 recites that the DMOS transistors **share in common either a source or a drain**. That is, in the array of claim 1 there is a single source (or drain) that is shared by N DMOS transistors.

Meanwhile, the text at col. 8, lines 26-30 of Williams discloses that FIG. 9B shows a circuit topology with "a high voltage common source p-channel pull-up device." That is, as would be well understood upon inspection of FIG. 9B by anyone of even basic skill in the broad field of electrical engineering, the p-channel pull-up transistor in FIG. 9B is connected in a **common source circuit configuration** (to be

distinguished from the pull-up transistor of FIG. 9A which is connected in a source follower circuit configuration – see col. 8, lines 26-30)!

Meanwhile, Williams never discloses or suggests with respect to FIG. 2 that N (or any number) of DMOS transistors **share in common either a source or a drain**. Indeed, FIG. 9B only shows two transistors – a p-channel pull-up transistor and an n-channel pull-down transistor. And, again, as anyone of even basic skill in the broad field of electrical engineering would understand, it is not possible for a p-channel pull-up transistor to share a common source or drain with an n-channel pull-down transistor!

Meanwhile, FIG. 7 of Williams, also cited in the Office Action, similarly fails to show N DMOS transistors laterally arranged in an epitaxial layer, wherein the N DMOS transistors share in common either a source or a drain.

Finally, FIG, 13 of Williams, also cited in the Office Action, appears to show **a** source region surrounding **a** (single) drain region. It does not show N DMOS transistors laterally arranged in an epitaxial layer, wherein the N DMOS transistors share in common either a source or a drain, as featured in claim 1.

Accordingly, for at least these reasons, Applicants respectfully submit that claim 1 is patentable over Williams.

Claims 2-3 and 16-20

Claims 2-3 and 16-20 depend from claim 1 and are therefore deemed patentable over Williams for at least the reasons set forth above with respect to claim 1, and for the following additional reasons.

Claim 2

In claim 2, the DMOS transistors laterally arranged in the epitaxial layer are N-type vertical double diffused MOS transistors (nVDMOS transistors).

Applicants respectfully submit that Williams fails to disclose an array including such a combination of features. In particular, the Office Action states that FIG. 7 discloses vertical DMOS devices. However, the vertical DMOS devices of FIG. 7: (1) are not laterally arranged in the epitaxial layer; and (2) do not share in common either

a source or drain.

Accordingly, for at least these additional reasons, Applicants respectfully submit that claim 2 is patentable over Williams.

Claim 16

Among other things, in the array of claim 16 one of the source or drain commonly shared among the N DMOS transistors surrounds the one of the source or drain of each double diffused MOS transistor formed unique to each DMOS transistor.

Applicants respectfully submit that no such feature is disclosed by Williams.

Accordingly, for at least these additional reasons, Applicants respectfully submit that claim 16 is patentable over Williams.

NEW CLAIM 21

Claim 21 depends from claim 1 and is deemed patentable for at least the reasons set for the above with respect to claim 1.

Also, among other things, the array of claim 21 includes at least 3 DMOS transistors laterally arranged in a epitaxial layer, wherein the at least 3 DMOS transistors share in common either a source or a drain.

Applicants respectfully submit that Williams does not disclose or suggest such a feature.

Accordingly, for at least these additional reasons, Applicants respectfully submit that claim 21 is patentable over Williams.

CONCLUSION

In view of the foregoing explanations, Applicants respectfully request that the Examiner reconsider and reexamine the present application, allow claims 1-21, and pass the application to issue. In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Kenneth D. Springer (Reg. No. 39,843) at (571) 283-0720 to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and

future replies to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17, particularly extension of time fees.

Respectfully submitted,

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By: _____

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